METHOD AND SYSTEM FOR DETECTING AND PERFORMING AUTOMATIC BANK SWITCHING FOR A FILTER COEFFICIENT RAM

Priority Claim

This application claims the benefit of United States Provisional Patent Application No. 60/392,293, filed June 27, 2002, entitled "METHOD AND SYSTEM FOR DETECTING AND PERFORMING AUTOMATIC BANK SWITCHING FOR A FILTER COEFFICIENT RAM," which is incorporated herein by reference.

Field of the Invention

The present invention relates to data transfer and storage in a video processing system.

Background of the Invention

With the advent of digital and high definition television broadcasting modern television signal processing systems are required to receive and display multiple formats of television broadcasts. Each format has unique signal qualities and is optimally processed by unique filter configurations. It is desirable for the program broadcaster to be able to switch between formats during the course of the broadcast. It is therefore necessary for the television signal processing system to be able recognize a change in broadcast format and change the filter configuration to optimally process the new format.

Changing the filter configuration during a broadcast can result in undesirable disturbances in the picture, such as video flashes, pairing in interlaced signals, loss of picture synchronization, or audio disturbances. It is advantageous to eliminate these undesirable disturbances and perform the switch in program formats smoothly so the viewer is unaware of any change.

Summary of the Invention

In one aspect, the present invention involves a method for managing memory in a video signal processing device comprising disabling a first memory and a second memory, switching an output from the first memory to the second memory in response to a portion of a video signal, and enabling the first memory and the second memory.

In another aspect, the invention also involves an apparatus for selecting one of a plurality of video filter coefficients comprising a first memory for storing a first set of video filter coefficients, a second memory for storing a second set of video filter coefficients, a switch for selecting either the first memory or the second memory, and a bank switching device for detecting a portion of a video signal and changing the state of the switch.

Brief Description of the Drawings

Figure 1 is a block diagram of a multiformat television signal processing systems,

Figure 2 is a block diagram of an exemplary implementation of a video format converter in a digital video receiving system.

Figure 3 is a block diagram of an exemplary implementation of memory bank switching circuitry.

Figure 4 is a flowchart that illustrates the process of detecting a program format change, the process of detecting a vertical blanking interval and the process of switching the video filter coefficients.

Detailed Description of the Preferred Embodiment

The characteristics and advantages of the present invention will become more apparent from the following description, given by way of example. One embodiment of the present invention may be included within an integrated circuit. Another embodiment of the present invention may comprises discrete elements forming a circuit.

FIG. 1 is a block diagram of an exemplary digital video receiving system (10) according to the present invention. System (10) includes an antenna (20) and an input processor (22) for together receiving and digitizing a broadcast carrier modulated with signals carrying audio, video, and associated data. System (10) also includes a demodulator (24) for receiving and demodulating the digital output from input processor (22). Further, system (10) includes a remote control unit (26) for receiving user input commands. System (10) also includes one or more digital-input-to-digital-output or digital-input-to-analog-output display driver(s) (28) and a respective digital-input or analog-input display (30) for together converting digital video picture data into visual representations. In the preferred embodiment, display (30) is a multiformat television display unit and, accordingly, display driver(s) (28) is a

suitable multiformat-input-to-digital-output device. While the present invention is described in regard to the exemplary embodiment of Figure 1 which includes a display device, the invention is also applicable to systems that do not include a display device such as set top boxes, video cassette recorders, and DVD players.

System (10) further includes a video processor (32). In general, video processor (32) receives user input commands from remote control unit (26), receives the demodulated data from demodulator (24), and transforms the demodulated data into video picture data for display driver(s) (28) in accordance with the user input commands. Accordingly, video processor (32) includes a remote interface (34) and a controller (36). Remote interface (34) receives user input commands from remote control unit (26). Controller (36) interprets the input commands and appropriately controls settings for various components of processor (32) to carry out the commands (e.g., channel and/or on-screen display ("OSD") selections). Video processor (32) further includes a decoder (38) for receiving the demodulated data from demodulator (24) and outputting a digital signal that is trellis decoded, mapped into byte length data segments, de-interleaved, and Reed-Solomon error corrected. The corrected output data from decoder (38) is in the form of a Moving Picture Experts Group ("MPEG") standard compatible transport data stream containing program representative multiplexed audio, video, and data components.

Processor (32) further includes a decode packet identifier ("PID") selector (40) and a transport decoder (42). PID selector (40) identifies and routes selected packets in the transport stream from decoder (38) to transport decoder (42). Transport decoder (42) digitally demultiplexes the selected packets into audio data,

video data, and other data for further processing by processor (32) as discussed in further detail below.

The transport stream provided to processor (32) comprises data packets containing program channel data, ancillary system timing information, and program specific information such as program content rating and program guide information. Using the program specific information, transport decoder (42) identifies and assembles individual data packets including the user selected program channel. Transport decoder (42) directs the ancillary information packets to controller (36) which parses, collates, and assembles the ancillary information into hierarchically arranged tables.

The system timing information contains a time reference indicator and associated correction data (e.g., a daylight savings time indicator and offset information adjusting for time drift, leap years, etc.). This timing information is sufficient for an internal decoder (e.g., MPEG decoder (44), discussed below) to convert the time reference indicator to a time clock (e.g., United States eastern standard time and date) for establishing a time of day and date of the future transmission of a program by the broadcaster of the program. The time clock is useable for initiating scheduled program processing functions such as program play, program recording, and program playback.

Meanwhile, the program specific information contains conditional access, network information, and identification and linking data enabling system (10) to tune to a desired channel and assemble data packets to form complete programs. The program specific information also contains ancillary program content rating

information (e.g., an age based suitability rating), program guide information (e.g., an Electronic Program Guide ("EPG")) and descriptive text related to the broadcast programs as well as data supporting the identification and assembly of this ancillary information.

System (10) also includes an MPEG decoder (44). Transport decoder (42) provides MPEG compatible video, audio, and sub-picture streams to MPEG decoder (44). The video and audio streams contain compressed video and audio data representing the selected channel program content. The sub-picture data contains information associated with the channel program content such as rating information, program description information, and the like. MPEG decoder (44) decodes and decompresses the MPEG compatible packetized audio and video data from transport decoder (42) and derives decompressed program representative data therefrom.

MPEG decoder (44) also assembles, collates and interprets the sub-picture data from transport decoder (42) to produce formatted program guide data for output to an internal OSD module (not shown). The OSD module processes the sub-picture data and other information to generate pixel mapped data representing subtitling, control, and information menu displays including selectable menu options and other items for presentation on display (30). The control and information displays, including text and graphics produced by the OSD module, are generated in the form of overlay pixel map data under direction of controller (36). The overlay pixel map data from the OSD module is combined and synchronized with pixel representative data from decoder (38) under the direction of controller (36). Combined pixel map data

representing a video program on the selected channel together with associated sub-picture data is encoded by MPEG decoder (44).

System (10) further includes one or more display processor(s) (46). In general, display processor(s) transform the encoded program and sub-picture data from MPEG decoder (44) into a form compatible with display driver(s) (28). In the exemplary embodiment, display processor(s) (46) include a video format converter ("VFC") (60) (see FIG. 2) according to the present invention as discussed further below.

FIG. 2 is a block diagram of an exemplary implementation of a video format converter ("VFC") (60) in a digital video receiving system according to the present invention. The VFC (60) includes a plurality of parallel video line memories (62), a VFC controller (64), a VFC filter (66), a filter coefficient RAM (70), and a first-in first-out ("FIFO") data buffer 68. The VFC (60) receives an input video stream (61) from the MPEG decoder (44) and transmits an output video stream (69) to the display processors (46). In general, VFC controller 64 controls video line memories (62) and the VFC filter (66) to store or queue data from an incoming video stream (61). Further, the video filter coefficient RAM (70) is configured to operate in response to the VFC controller (64) to make the optimal set of video filter coefficients available to the VFC filter (66) for the display format being processed by the display processor (46).

A change in the display format of the incoming video stream requires a change in the video filter coefficients being used by the VFC filter (66) to produce the best possible picture. However, changing the video filter

coefficients may result in undesirable disturbances in the output video stream, and subsequently the picture, such as video flashes, pairing in interlaced signals, loss of picture synchronization, or audio disturbances. It is advantageous to eliminate these undesirable disturbances and perform the switch in program formats smoothly so the viewer is unaware of any change. When the VFC controller (64) determines that a change in display format of the incoming video stream has occurred, the VFC controller (64) transmits the addresses of the video filter coefficients for the new display format to the video filter coefficient RAM (70). After receiving the complete set of addresses for the video filter coefficients of the new display format from the VFC controller (64), the filter coefficient RAM (70) then makes a transition between the video filter coefficient sets of the previous display format and the new display format during a subsequent vertical blanking interval.

A television video signal includes video intervals alternating with blanking intervals where the video is interrupted so that display (30) scan beam can be quickly returned to a point where a subsequent scan is commenced. There are two types of blanking intervals, the horizontal blanking interval which occurs once for each line of the video image and which contains a single horizontal sync pulse, and the vertical blanking interval which occurs after each field of video information. The vertical blanking interval generally includes six relatively wide vertical synchronization pulses preceded by six relatively narrow pre-equalization pulses and followed by six relatively narrow post-equalization pulses. After the

filter coefficient RAM (70) senses the vertical synchronization pulses, it initiates the transition between the video filter coefficient sets of the previous display format and the new display format. Since the transition is made during a vertical blanking interval, when there is no video output, the transition is in a manner to prevent undesirable disturbances in the picture.

FIG. 3 is a block diagram of an exemplary embodiment of the filter coefficient RAM (70) including an apparatus to control the switching of memory banks storing video filter coefficients. The system shown in Figure 3 includes a register bus (370), coefficient address detector (310), a bank switching state machine (340), a first input multiplexer (410) and second input multiplexer (411), a first RAM (418) and a second RAM (419) and an output multiplexer (422). A portion of the register bus (370) includes an address bus (403,404,408,409). The register bus (370) can be accessed by the the VFC Controller (64, Fig.2), the coefficient address detector (310), the VFC filter (66, Fig. 2), the first input multiplexer (410) and the second input mutiplexer (411) and is used to read and write the banks of filter coefficients that are used by the VFC filter (66, Fig.2).

The VFC controller (64, Fig.2) writes the addresses to the RAM (418, 419) selected at that time to be in the write mode. This selection is made via the bank select line (350) from the bank switching state machine (340). It should be noted that only one input multiplexer (410,411) can be configured to be in the write mode at any one time as the other input multiplexer (410,411) operates on the inverse of the bank select line (350). Therefore when the bank select line is high, for example, the first input multiplexer (410) is in the write mode, while the second input multiplexer (411)

other is in the read mode. When the state of the bank select line (350) changes state, the function of each input multiplexer (410,411) changes in response, thus the first input mutiplexer (410) is in the read mode while the second input multiplexer (411) is in the write mode. Therefore, only one RAM (418,419) can be written to at one time and only one RAM (418,419) can be read from at any one time, dependant on the state of the bank select line (350).

The VFC filter (66, Fig. 2) requests the address of the video filter coefficients currently required from the RAM (418,419) via the read address line (403,408) of the input multiplexer (410,411) currently in the read mode. The requested address information is then read via the bank data line (424) connected to the VFC filter (66, Fig. 2).

The address detector (310) monitors the data on the register bus (370) to determine the status of writing addresses to the RAMs by the VFC controller (64, Fig. 2). When the address detector (310) detects addresses of filter coefficients being written a RAM (418,419), which indicates a change in the format of the incoming video stream (61, Fig. 2), the address detector (310) determines when the last address of the filter coefficient has been written, either by counting the number of addresses written and comparing that number against a known quantity or by an alternate method, and then sets the last_addr_written flag to the bank switching circuitry (340). The last_addr_written flag is set by changing the state of the last flag written line (320) connecting the coefficient address detector (310) and the bank switching circuitry (340). After observing the "last_addr_written" flag, the bank switching circuitry (340) monitors the vertical blanking line (330) for the next vertical

blanking interval, which is indicated by a vertical sync pulse associated with the input video stream as described previously.

After the vertical blanking interval is indicated, the bank switching circuitry, (340) disables the RAMS (418,419) via the chip enable/disable line (350) to prevent false reads or writes from occurring. A false read or write may occur when information is being read from the RAM (418,419) and written to the RAM (418, 419) at the same time. In this instance, the VFC filter (66, Fig. 2) may erroneously read video filter coefficients from both the new set of video filter coefficients being written and the set being written over, thereby resulting in an incorrect set of video filter coefficients. Additionally, similar errors may also occur with a single address being read and written at the same time. After the RAMS (418,419) are disabled, the bank switching circuitry (340) switches the RAM (418,419) to be read via the bank select line (350) as described previously. The bank select line (350) concurrently is used to switch the state of the input multiplexers. (410,411) Switching the state of the input multiplexers. (410,411) connects the read clock (401) and read address (403) lines to the RAM (418,419) previously set to write and connects the write clock and write address lines (416) the RAM (418,419) previously set to read. The input multiplexers are connected to the RAMS (418,419) via conductive lines. (414, 416) After the bank switching circuitry (340) changes the state of the bank select line (350) it enables the RAMS (418,419) via the chip enable/disable line. (350) At this time, the video filter coefficients for the new video format are able to be read by the VFC filter (66, Fig 2) via the bank data line (424) and the output multiplexer (422).

Figure 4 is a flowchart illustrating the process of detecting a program format change, the process of detecting a vertical blanking interval and the process of switching the video filter coefficients according to the following exemplary memory management technique of the present invention:

1. The coefficient address detector (310) monitors the register bus to determine if new addresses are being written by the VFC controller (64) to the RAMs (418,419).
2. After the coefficient address detector (310) determines new addresses are being written, indicating a change in the input video format, the coefficient address detector (310) monitors the addresses being written to determine when the last address has been written.
3. After the last address has been written by the VFC controller, the coefficient address detector (310) sets the last_addr_written flag (320).
4. When the bank switching state machine (340) observes the last_addr_written flag, it monitors the vertical blanking line (330) to determine the start of the next vertical blanking period.
5. After the next vertical blanking period is indicated via the vertical blanking line (330), the bank switching state machine (340) disables the RAMs (418,419) via the enable disable line (350).
6. The bank switching state machine (340) then switches the read/write functions of the RAMs (418,419) via the bank select line (350).

7. The bank switching state machine (340) then enables the RAMs (418,419) via the via the enable disable line (350).
8. The address detector then returns to the initial state of monitoring the register bus to determine if new addresses are being written by the VFC controller (64) to the RAMs (418,419).

While the present invention has been described with reference to the preferred embodiments, it is apparent that various changes may be made in the embodiments without departing from the spirit and the scope of the invention, as defined by the appended claims.